PRELIMINARY

Technical Information Manual

Revision n. 0

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MOD. V1742

32+2 CH 12 BIT
5 GS/s DIGITIZER
MANUAL REV.0

NPO:
00103/09:V1742x.MUTx/00

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1. General description

1.1. Overview

The Mod. V1742 is a VME board housing two 16+1Channels 12bit 5GS/s Switched Capacitor Digitizer sections, based on DRS4 (Domino Ring Sampler) chip, with 1 Vpp input dynamic range on single ended MCX coaxial connectors. A VME64X mechanics version, Mod. VX1742 is also available.

The DC offset is adjustable via 16bit DAC (± 1V range) on each channel and allows tot sample either bipolar (Vin=± 0.5V) or unipolar (full positive Vin= 0 ÷ +1V or negative Vin= 0 ÷ -1V) analog input swing without losing dynamic resolution.

The analog input signals are continuously sampled into the DRS4s in a circular analog memory buffer (1024 cells); default sampling frequency is 5GS/s; 2.5GS/s and 1GS/s frequencies can be also programmed. As a trigger signal arrives, all analog memory buffers are frozen and subsequently digitized with a 12bit resolution into a digital memory buffer. The digital memory (128 events deep for each channel, where 1 event = 1024x12bit) allows to store subsequent events, even if the readout is not yet started.

Moreover, since the digital memory buffers work like FIFOs, the readout activity from VME or Optical Link does not affect write operations of subsequent events.

A common board trigger can be provided via VME or Optical Link, or by TRG-IN input.

Two special fast analog trigger inputs TR0 and TR1 (TTL/NIM levels compatible), can be used as lo-latency external trigger signals. These special inputs can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required.

During analog to digital conversion process, the V1742 cannot handles other triggers, this is called Dead Time. Dead time will be increased if also TR0 and/or TR1 channels are sampled in the acquisition of the analog inputs.

The module V1742 features a PLL for clock synthesis with a selectable internal or external reference clock source.

Multi-board synchronization can be done by driving a clock on CLOCK-IN input, allowing all DRS4s to run synchronously with this external reference. All analog inputs will be sampled at the same time without time drift, allows high resolution timing and time analysis across multiple V1742.

The Modules VME interface is VME64X compliant and the data readout can be performed in Single Data Transfer (D32), 32/64 bit Block Transfer (BLT, MBLT, 2eVME, 2eSST) and 32/64 bit Chained Block Transfer (CBLT).

The board houses a daisy chainable Optical Link able to transfer data at 80 MB/s, thus it is possible to connect up to 8 ADC boards (256+16 ADC channels) to a single Optical Link Controller (Mod. A2818). Optical Link and VME access are internally arbitrated.

Table 1.1: Mod. V1742 versions

Model	Code	SRAM Memory	Form factor
V1742	WV1742BXAAAA	128 event / ch	6U-VME64
V1742B	WV1742XAAAAA	1024 event / ch	6U-VME64
VX1742	WVX1742BXAAA	128 event / ch	6U-VME64X
VX1742B	WVX1742XAAAA	1024 event / ch	6U-VME64X

1.2. Block Diagram

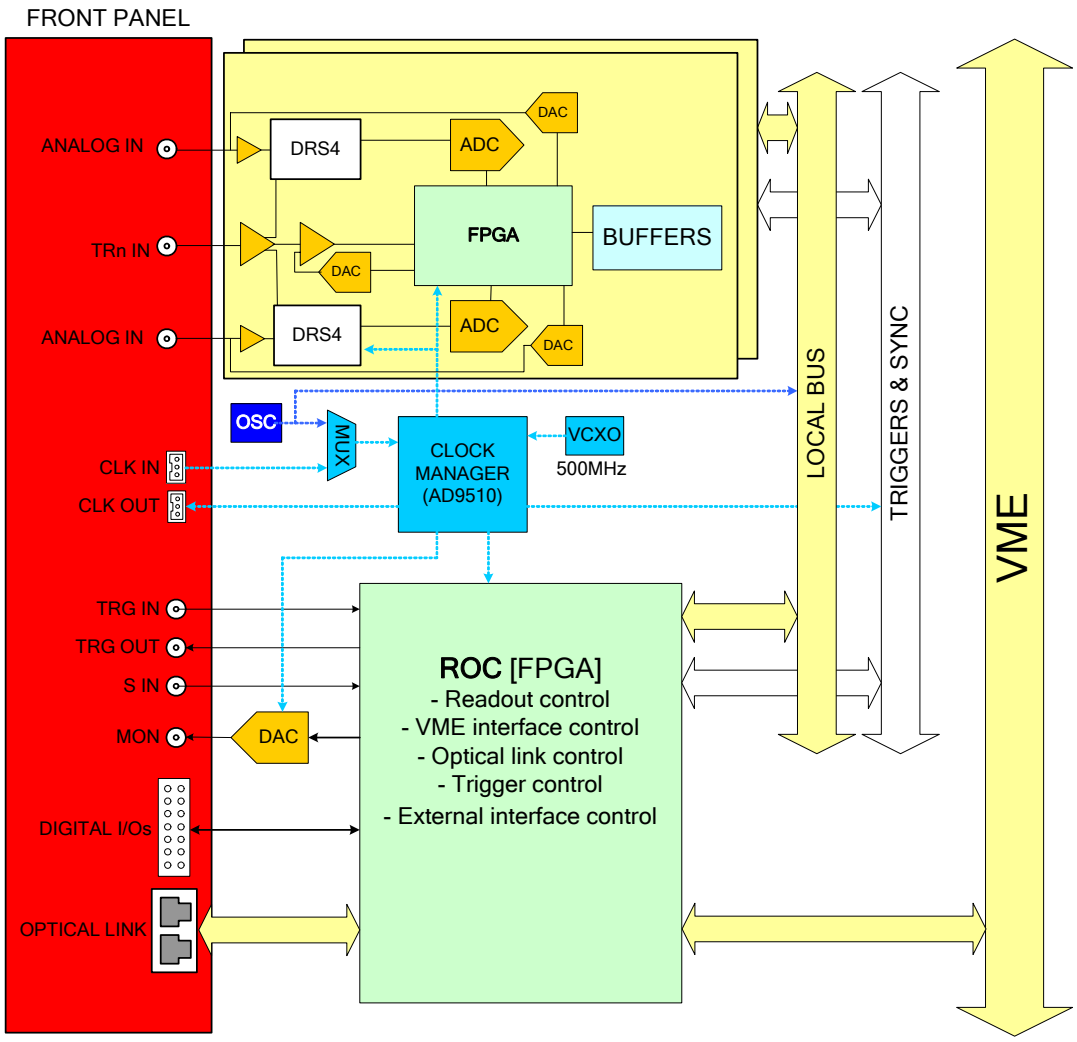

Fig. 1.1: Mod. V1742 Block Diagram

The function of each block will be explained in detail in the subsequent sections.

2. Technical specifications

2.1. Packaging and Compliancy

The module is housed in a 6U-high, 1U-wide VME unit. The board hosts the VME P1, and P2 connectors and fits into both VME/VME64 standard and V430 backplanes. VX1742 versions fit into VME64X compliant crates. In all cases only well ventilated crates must be used.

2.2. Power requirements

The power requirements of the module are as follows:

Table 2.1: Model V1742 power requirements

+5 V	5.5 A
+12 V	200 mA
-12 V	300 mA

2.3. Front Panel

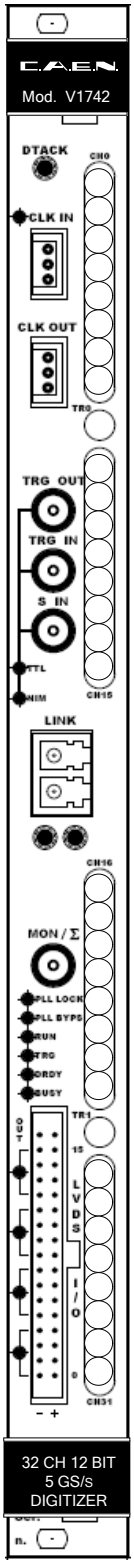

Fig. 2.1: Mod. V1742 front panel

2.4. External connectors

2.4.1. INPUT connectors

Fig. 2.2: MCX connector

Function:
Analog input, single ended, Zin=50 Ohm; TR[1,0] (Fast TRG) input, Zin=50 Ohm
Mechanical specifications:
MCX connector (CS 85MCX-50-0-16 SUHNER)
Suggested plug: MCX-50-2-16 type
Suggested cable: RG174 type

2.4.2. CONTROL connectors

Function:
- TRG OUT: Local trigger output (NIM/TTL, on Rt = 50 Ohm)
- TRG IN: External trigger input (NIM/TTL, Zin= 50 Ohm)
- SYNC/SAMPLE/START (S_IN): Sample front panel input (NIM/TTL, Zin=50 Ohm)
- MON/Σ: DAC output 1Vpp on Rt=50 Ohm

Mechanical specifications: 00-type LEMO connectors

2.4.3. ADC REFERENCE CLOCK connectors

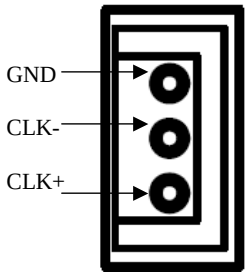

Fig. 2.3: AMP CLK IN/OUT Connector

CLK_IN
Function: CLK IN: External clock/Reference input, AC coupled (diff. LVDS, ECL, PECL, LVPECL, CML), Zdiff= 100 Ohm.
Mechanical specifications: AMP 3-102203-4 connector
CLK_OUT
Function: CLOCK OUT: Clock output, DC coupled (diff. LVDS), Zdiff= 100 Ohm.
Mechanical specifications: AMP 3-102203-4 connector

2.4.4. Digital I/O connectors

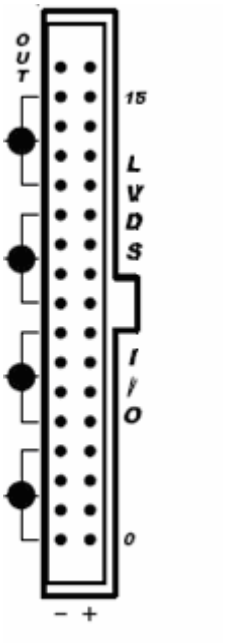

Fig. 2.4: Programmable IN/OUT Connector

Function: N.16 programmable differential LVDS I/O signals, Zdiff_in= 110 Ohm. Four Independent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control;
Lowest couple: 0; highest couple: not connected. See also § 3.8.
Mechanical specifications: 3M-7634-5002- 34 pin Header Connector

2.4.5. Optical LINK connector

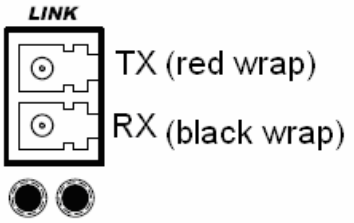

Fig. 2.5: LC Optical Connector

Mechanical specifications: LC type connector; to be used with Multimode 62.5/125µm cable with LC connectors on both sides (see also § 3.14); CAEN provides optical fiber cables with a duplex connector on the A2818 side and two simplex connectors on the board side; the simplex connector with the black wrap is for the RX line (lower) and the one with the red wrap is for the TX (higher).
Electrical specifications: Optical link for data readout and slow control with transfer rate up to 80MB/s; TX/RX, daisy chainable.

2.5. Other front panel components

2.5.1. Displays

The front panel hosts the following LEDs:

Table 2.2 : Front panel LEDs

Name:	Colour:	Function:
DTACK	green	VME read/write access to the board
CLK_IN	green	External clock enabled.
NIM	green	Standard selection for CLK I/O, TRG OUT, TRG IN, S IN.
TTL	green	Standard selection for CLK I/O, TRG OUT, TRG IN, S IN.
LINK	green/yellow	Network present; Data transfer activity
PLL _LOCK	green	The PLL is locked to the reference clock
PLL _BYPS	green	The reference clock drives directly ADC clocks; the PLL circuit is switched off and the PLL_LOCK LED is turned off.
RUN	green	RUN bit set (see § 4.24)
TRG	green	Trigger accepted
DRDY	green	Event/data (depending on acquisition mode) are present in the Output Buffer
BUSY	red	All the buffers are full
OUT_LVDS	green	Signal group OUT direction enabled.

2.6. Internal components

SW2,4,5,6 “Base Addr. [31:16]”: *Type:* 4 rotary switches
Function: Set the VME base address of the module.

SW3 “CLOCK SOURCE”: Type Dip Switch
*Function:*Not Used

SW1 “FW”: Type: Dip Switch.
Function: it allows to select whether the “Standard” (STD) or the “Back up” (BKP) firmware must be loaded at power on; (default position: STD).

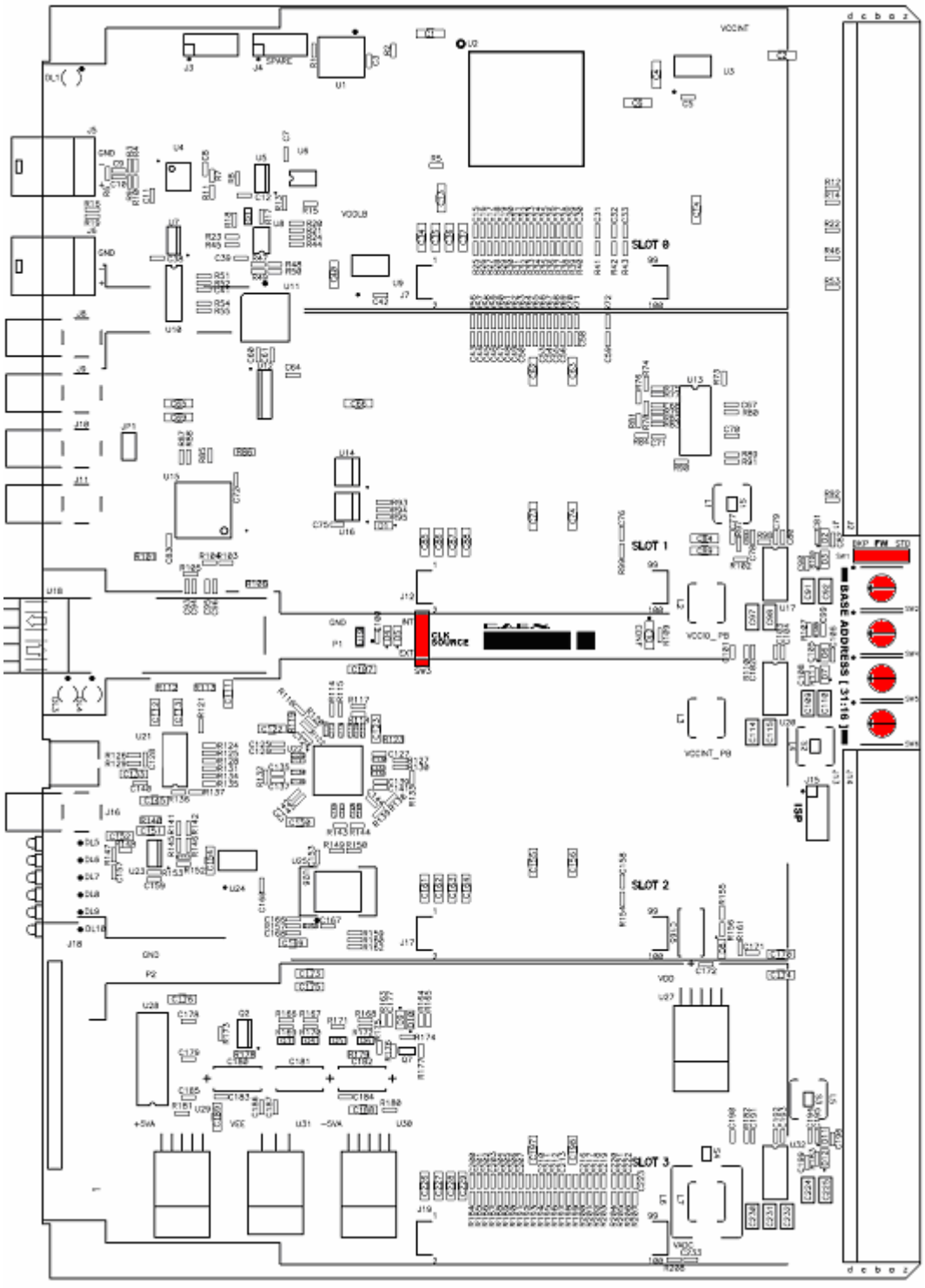

Fig. 2.6: Rotary and dip switches location

2.7. Technical specifications table

Table 2.3 : Mod. V1742 technical specifications

Package	1-unit wide VME module
Analog Input	32 channels (MCX 50 Ohm); Single-ended; Input range: 1 Vpp Bandwidth: >500MHz; Programmable DAC for Offset Adjust x ch. adjustment range: ±1V
Sampling frequency	Programmable: 5, 2.5 or 1GS/s
TR0, TR1 Input	MCX 50 Ohm, NIM/TTL; fast local trigger (TR0 for ch0..15, TR1 for ch16..31) and high resolution timing reference
Switched Capacitor array	Based on DRS4 chip Switched capacitor ADC 1024 storage cells per channels simultaneously sampled at 5 - 2,5 - 1GS/s (selectable) on all channels After trigger analog samples are digitized by external ADC.
Digital Resolution	12 bit
Dead Time	110µs Analog inputs only; 181µs Analog inputs + TR0, TR1 inputs
ADC Sampling Clock generation	sampling clock generation supports two operating modes: PLL mode - internal reference (50 MHz local oscillator) PLL mode - external reference on CLK_IN (Jitter<100ppm, Freq. 50 MHz).
Digital I/O	CLK_IN (AMP Modu II): AC coupled differential input clock LVDS, ECL, PECL, LVPECL, CML (single ended NIM/TTL available on request) Jitter<100ppm TRG_IN (LEMO 50 Ohm, NIM/TTL) S_IN (LEMO 50 Ohm, NIM/TTL)
ADC & Memory control FPGA	1 Altera Cyclone EP3C16 for 16+1 channels
Memory Buffer	128 event/ch, (1024 samples per event); Multi Event Buffer with independent read and write access.
Trigger	Common Trigger TRG_IN (External signal) Software (from VME or Optical Link) Fast local trigger Fast local trigger TR0 and TR1 with individual programmable analog threshold
Optical Link	CAEN proprietary protocol, up to 80 MB/s transfer rate, Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller (Mod. A2818/A3818)
Multi Modules Synchronization	Allows data alignment and consistency across multiple V1742 modules: CLK_IN allows the synchronization to a common clock source S_IN ensures start acquisition times alignment
Upgrade	Firmware can be upgraded via VME/Optical Link
VME interface	VME64X compliant D32, BLT32, MBLT64, CBLT32/64, 2eVME, 2eSST, Multi Cast CyclesTransfer rate: 60MB/s (MBLT64), 100MB/s (2eVME), 160MB/s (2eSST). Sequential and random access to the data of the Multi Event Buffer. The Chained readout allows to read one event from all the boards in a VME crate with a BLT access.
Software	Libraries (C and LabView), Demos and Software tools for Windows and Linux

3. Functional description

3.1. Analog input stage

Input dynamic is 1Vpp on single ended MCX coaxial connectors (Zin= 50 Ohm). A 16bit DAC allows to add up to ±1V DC offset in order to preserve the full dynamic range also with uni-polar positive or negative input signal. The input bandwidth ranges from DC to 500 MHz.

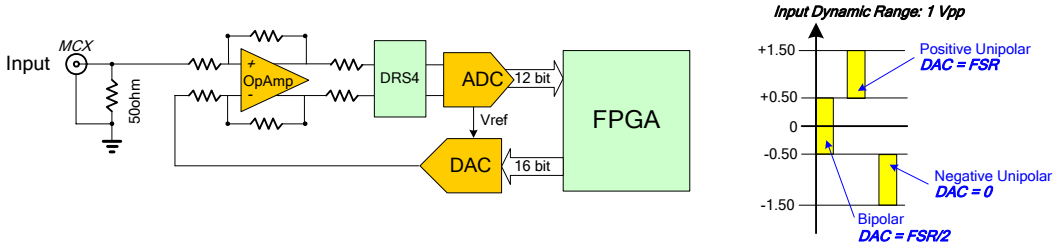

Fig. 3.1: Analog input diagram

3.2. Domino Ring Sampling

The analog input signals are continuously sampled into the DRS4s (Domino Ring Sampler), which consists of an on-chip inverter chain (domino wave circuit) generating a maximum 5GS/s sampling frequency; 2.5GS/s and 1GS/s frequencies can be also programmed (see § 4.21). No external sampling clock is required.

This signal opens write switches in all 9 sampling channels, where the differential input signals are sampled (1024 sampling capacitance cells per channel).

After being started, the domino wave runs continuously in a circular fashion (after the end of the ring, samples are over written) until decoupled from the write switches by a trigger signal, which freezes the currently stored signal in the sampling capacitance cells.

Subsequently the cells are multiplexed into the 12 bit ADCs whose output are stored by the FPGA into the Digital Memory Buffer and ready for readout in the shape of events data.

A 16bit DAC allow to add up to ±1V DC offset in order to preserve the full dynamic range also with uni-polar positive or negative input signals

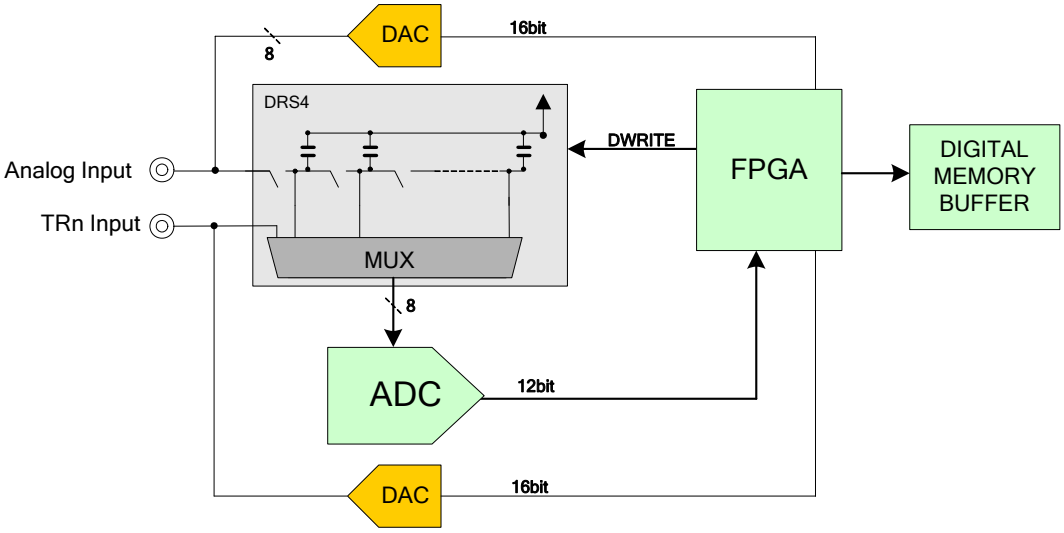

Fig. 3.2: Input diagram

Detailed documentation of the DRS4 is available at http://drs.web.psi.ch/

3.3. TR0 and TR1 Inputs

The module features two fast trigger inputs TR0 and TR1 with extended level amplitude (TTL/NIM compatible); TR0 is common to group 0 (ch[7..0]) and 1 (ch[15..8]), TR1 to group 2 (ch[23..16]) and 3 (ch[31..24]). TRn signals can be used as external triggers (see § 3.7). Moreover they can be also sampled into the DRS4s analog memory buffers for applications where high resolution timing and time analysis with a common reference signal (like a trigger or system clock) is required; this is achieved through the Configuration Register, “Signal TRn Readout Enable” bit setting (see § 4.12) allows to store TR0 input with samples coming from group 0 and 1 and TR1 with those from group 2 and 3.

To properly handle bipolar signals and also unipolar positive or negative signal, a 16 bit DAC allow you to add a DC offset to TRn; offset value can be programmed via Group n DC Offset register (see § 4.7)

When the TRn signals are used as trigger, they are processed by an internal comparator, whose threshold can be programmed via Group n TRn Threshold register (see § 0): as the threshold is exceeded, the FPGA triggers the DRS4’s and samples digitizing takes place. The trigger signals can be sensed either on the leading or the trailing edge, depending on Configuration register setting (see § 4.12).

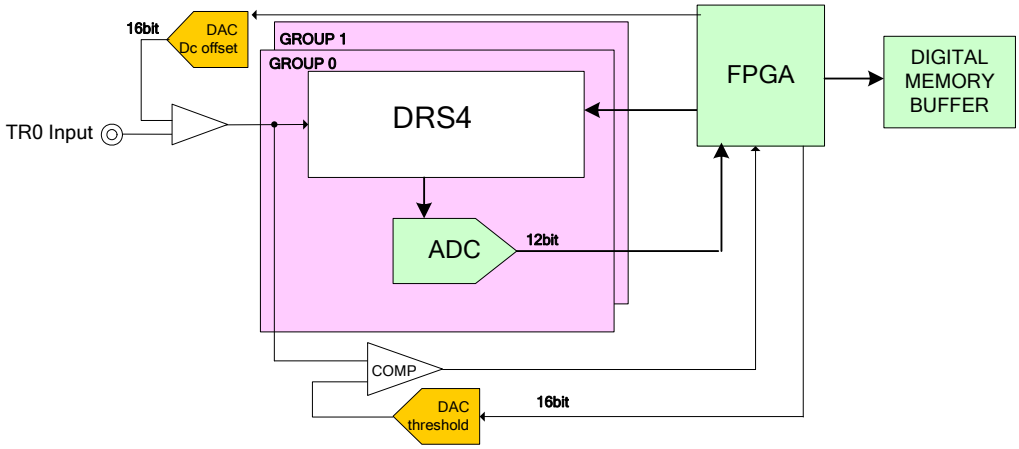

Fig. 3.3: TR0 logic block diagram

3.4. Clock Distribution

The module V1742 features a PLL for clock synthesis with a selectable internal or external reference clock source.

Multi-board synchronization can be done by driving a clock on CLOCK-IN input, allowing all DRS4s to run synchronously with this external reference. All analog inputs will be sampled at the same time without time drift, allows high resolution timing and time analysis across multiple V1742.

The module clock is provided by OSC-CLK and REF-CLK.
OSC-CLK is a fixed 50MHz clock provided by an on board oscillator; it handles both VME and Local Bus (communication between motherboard and mezzanine boards; see red traces in the figure below).
REF-CLK handles trigger logic, acquisition logic (samples storage into RAM, buffer freezing on trigger) through a clock chain. Such domain can use either an external (via front panel signal) or an internal (via local oscillator) source (selection is performed via dip switch SW1, see § 2.6); in the latter case OSC-CLK and REF-CLK will be synchronous (the operation mode remains the same anyway).
REF-CLK is processed by AD9510 device, which delivers 6 clock out signals; 4 signals are sent to ADCs, one to the trigger logic and one to drive CLK-OUT output (refer to AD9510 data sheet for more details, available on http://www.analog.com/

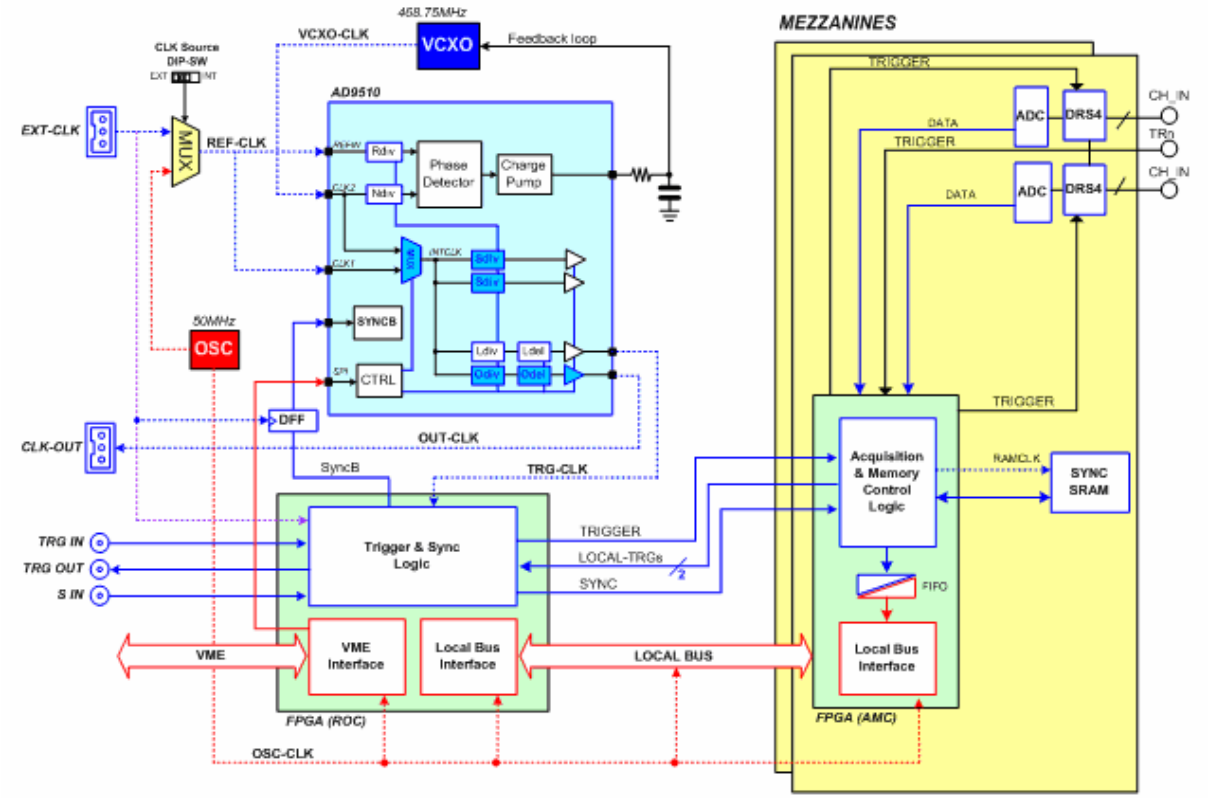

Fig. 3.4: Clock distribution diagram

3.4.1. Multi-board synchronization

To be implemented

3.5. Data correction

Three types of data correction are required, in order to compensate for unavoidable construction differences in the DRS4 chips. All boards are factory calibrated during production test and correction parameters are saved on board (see § 5.3). Application software provided by CAEN recovers automatically the calibration parameters and runs them in order to correct the stored data events.

3.5.1. Cell offset correction

Unavoidable construction differences between the "analog memory cells" (see § 3.1) require an amplitude calibration algorithm.
The following images show the sampled waveform and noise histogram before and after correction:

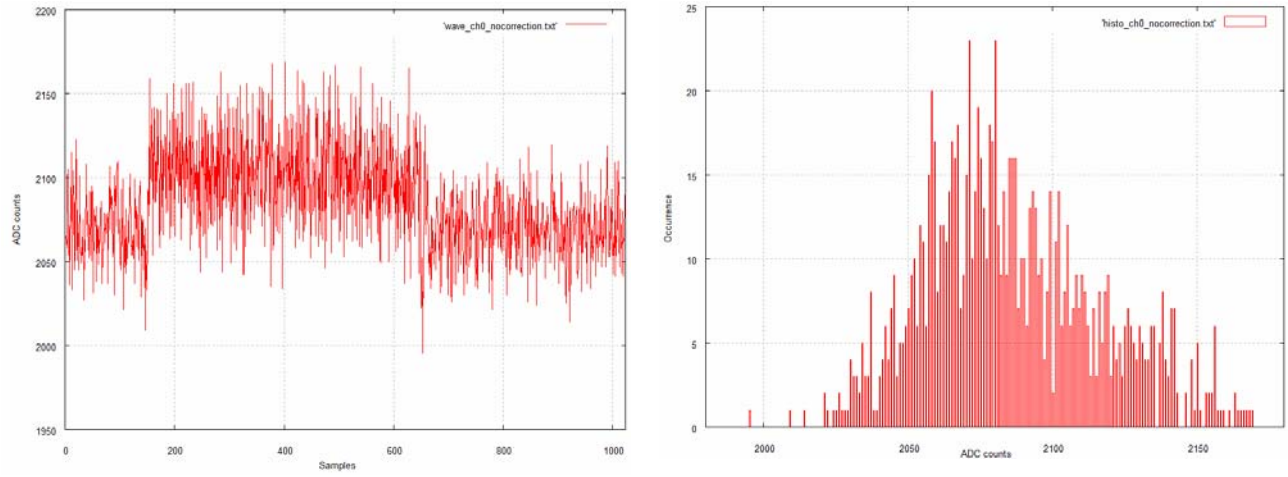

Fig. 3.5: Sampled waveform and noise histogram before cell offset correction

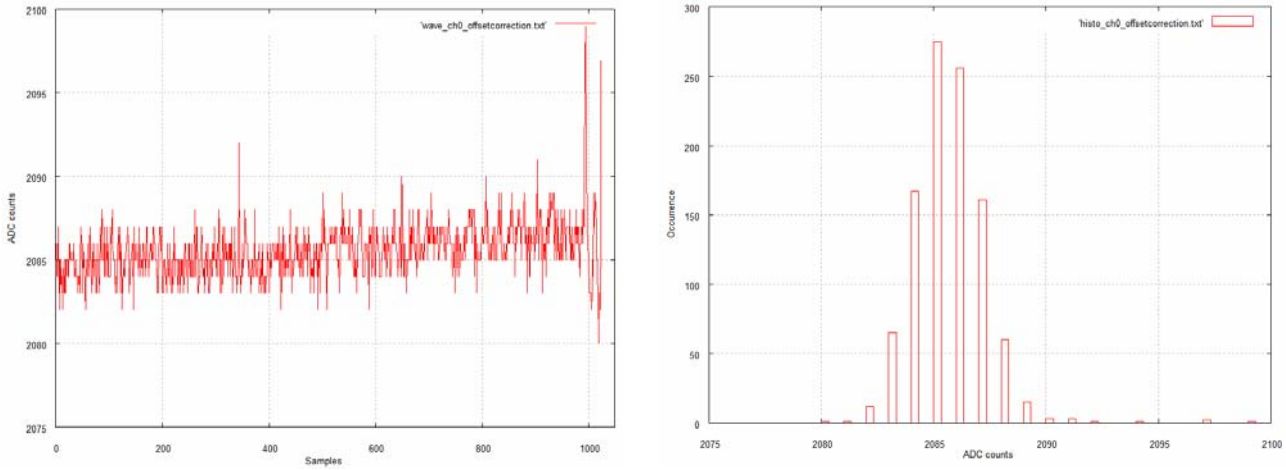

Fig. 3.6: Sampled waveform and noise histogram after cell offset correction

3.5.2. Index sampling correction

It has been observed a fixed pattern noise, introduced by the DRS4, over the last samples (~30 samples) in a waveform, therefore the "index sampling correction" is necessary; this correction actually reduces this noise, thus, anytime the best accuracy is required, the last ~30 samples should be rejected.

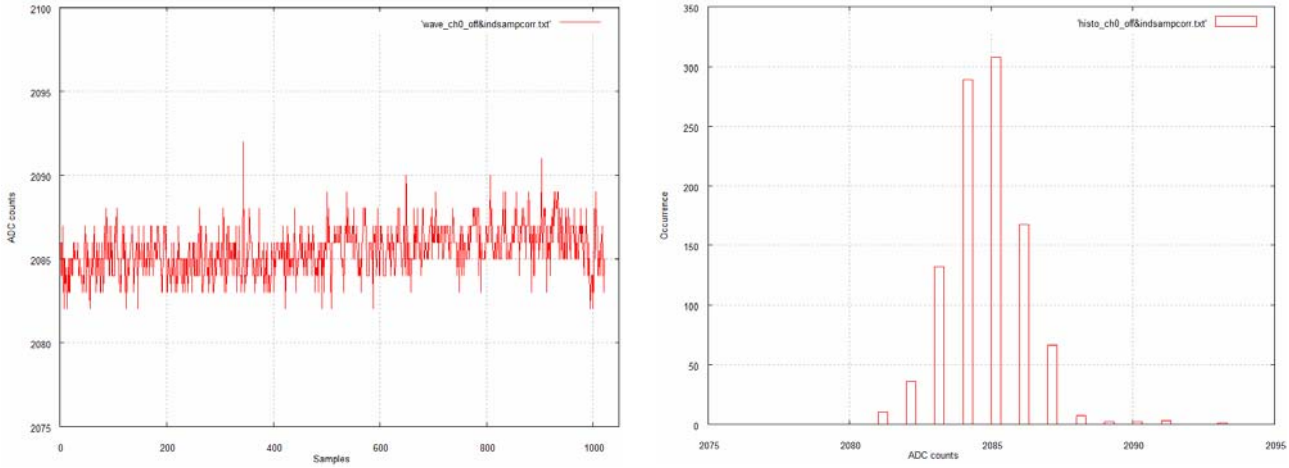

Fig. 3.7: Sampled waveform and noise histogram after index sampling correction

3.5.3. Time correction

The sampling sequence is handled by the DRS4 through 1024 physical delay lines; the unavoidable construction differences between such delay lines must be compensated through a time calibration. The following figures show the fast trigger signal (TR0) sampled by the DRS chip related to Group 0 and 1 and the integral non linearity (INL) time profile of DRS chips, before and after correction:

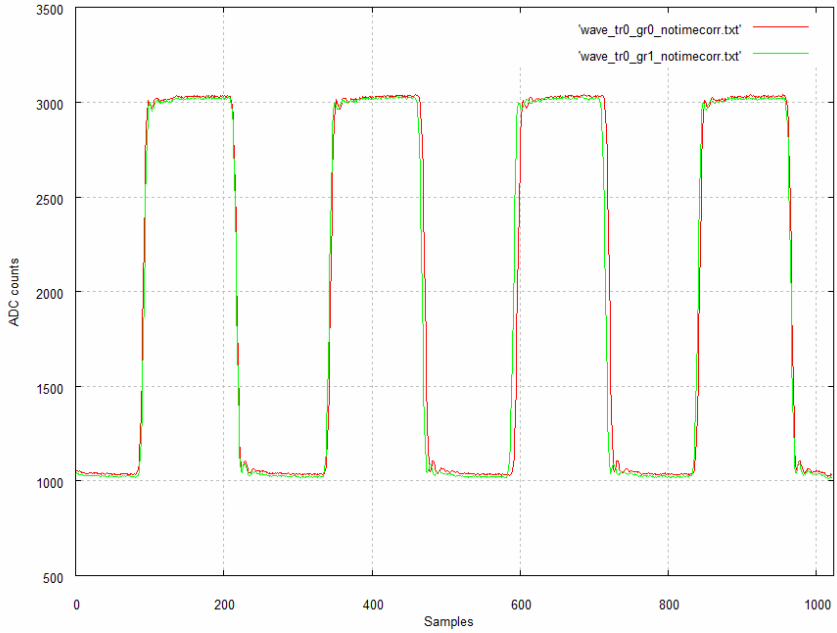

Fig. 3.8: Sampled TR0 signal in GR0 and GR1 before time correction

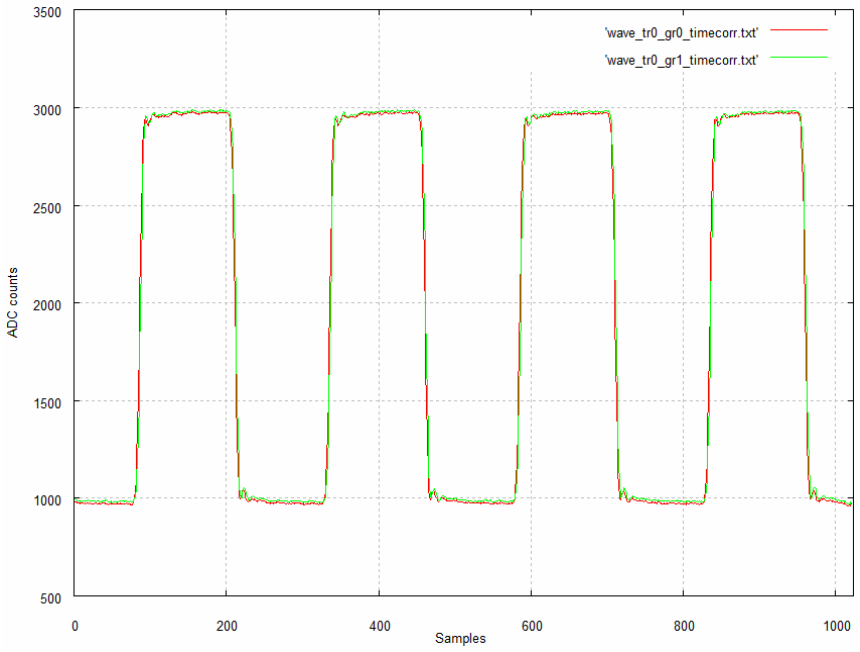

Fig. 3.9: Sampled TR0 signal in GR0 and GR1 after time correction

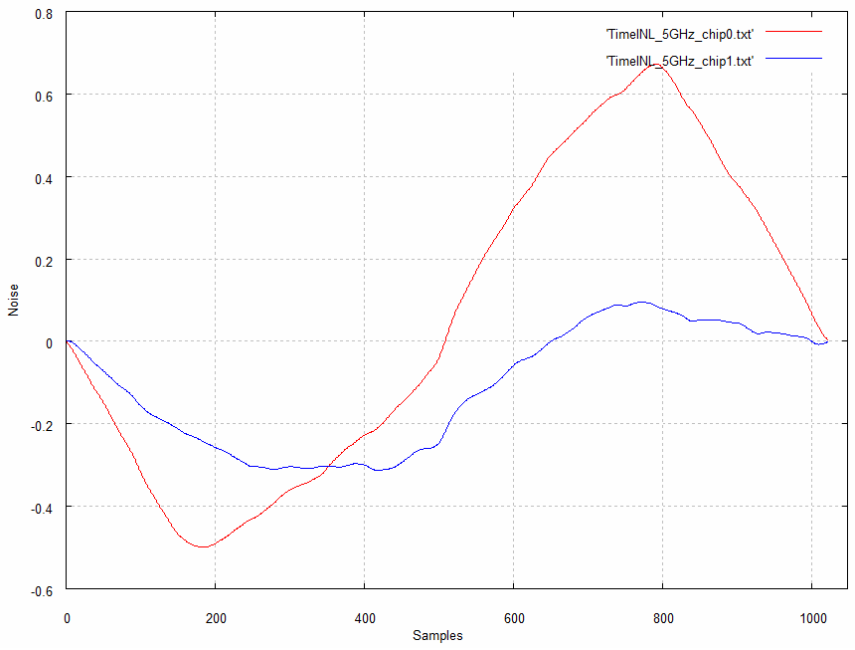

Fig. 3.10: INL time profile of DRS chips 0 and 1 before time correction

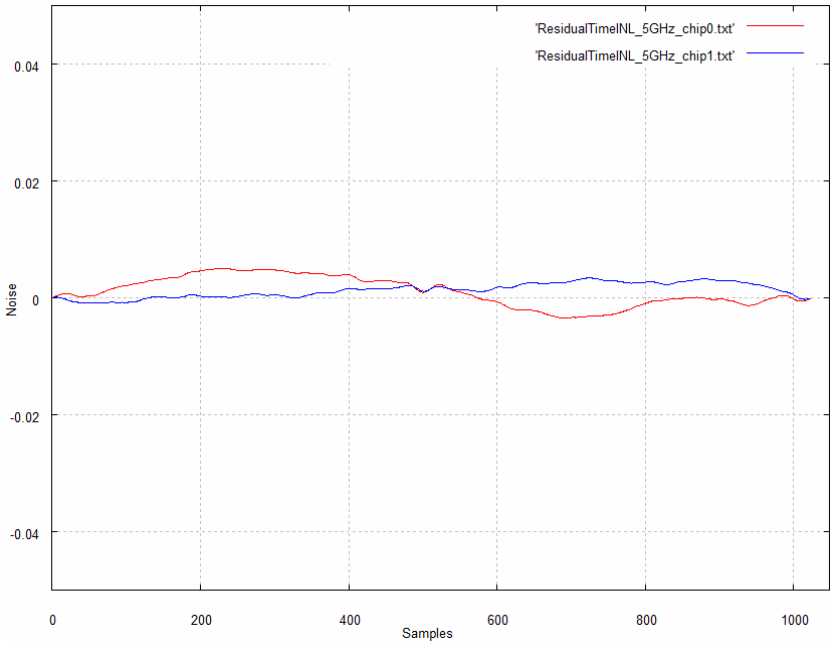

Fig. 3.11: INL time profile of DRS chips 0 and 1 after time correction

3.6. Event structure

An event is structured as follows:
- Header (four 32-bit words)
- Data (variable size and format)

The event can be readout either via VME or Optical Link; data format is 32 bit word.

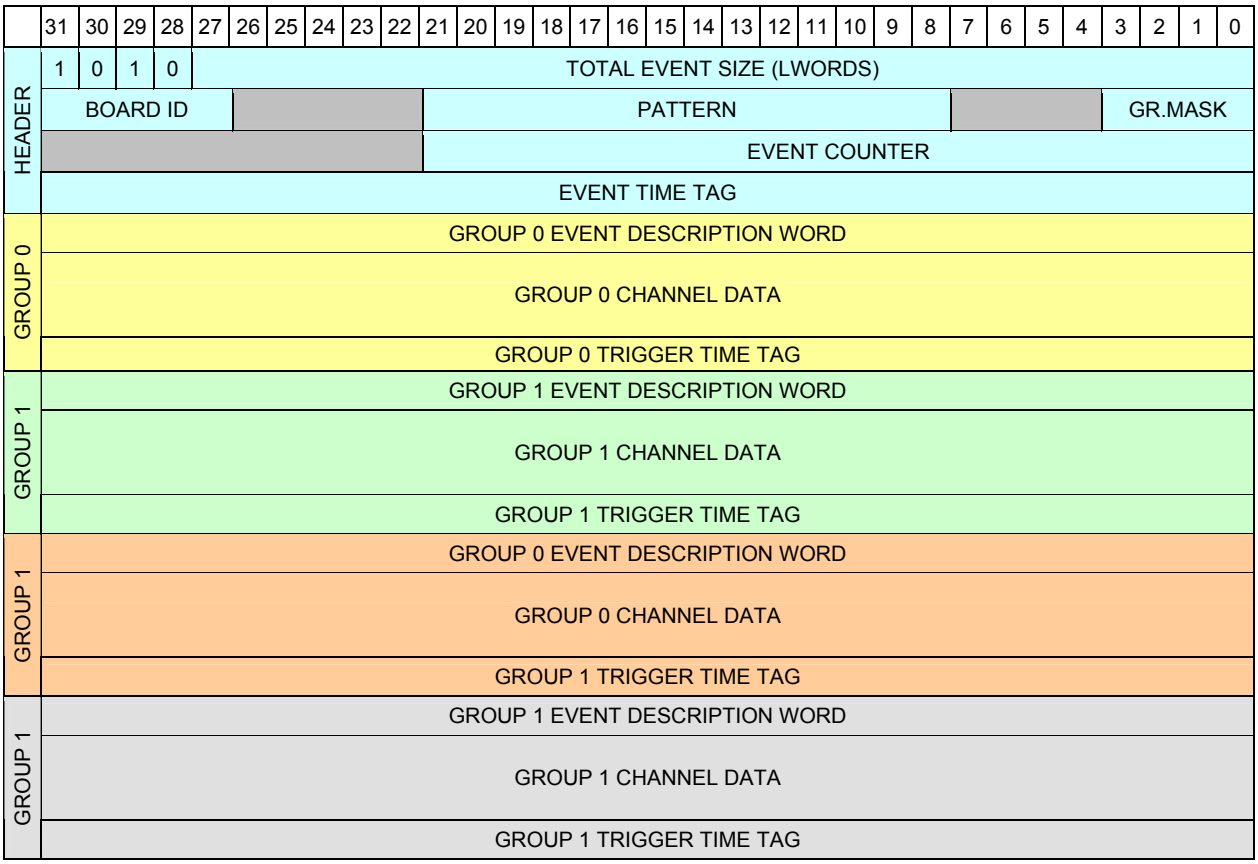

Fig. 3.12: Event Format

The Header is composed by four words, namely:
- Size of the event (number of 32 bit words)
- Board ID (GEO); 16 bit pattern, latched on the LVDS I/O as one trigger arrives; Group Mask (=1: Groups participating to event; ex GR2 and GR3 participating → Gr_Mask: 0xC, this information must be used by the software to acknowledge what Group the samples are coming from; the first event contains the samples from the Group with the lowest number)
- Event Counter: It is the trigger counter; it can count either accepted triggers only, or all triggers (see § 4.20).
- Trigger Time Tag: It is a 32 bit counter (31 bit count + 1 overflow bit), which is reset either as acquisition starts or via front panel Reset signal (see § 0), and is incremented at each sampling clock hit. It is the trigger time reference.

Each group is composed by 8 analog channels (group 0 = channel 0 – 7, group 1 = channel 8 – 15 etc.) and by the special channel TRn: such signal is common to two groups; it can be used as Local Trigger or “digitized” and stored with the data for high resolution timing analysis between the ADC channels and the TRn itself.

TR0 can trigger Group 0 and Group 1 and can be stored with data from Group 0 (therefore the stored waveform will be labelled as Tr00) and with data from Group 1 (therefore the stored waveform will be labelled as Tr01); TR1 can trigger Group 2 and Group 3 and can be stored with data from Group 2 (therefore the stored waveform will be labelled as Tr12) and with data from Group 3 (therefore the stored waveform will be labelled as Tr13).

The part of an event related to each group has the following format (example of Group 0):

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	START INDEX CELL										0	0	FREQ		0	0	0	TR	SIZE CH 0..7											
S0-CH2 (LO)								S0-CH1												S0-CH0											
S0-CH5(LO)								S0-CH4								S0-CH3												S0-CH2(HI)			
S0-CH7												S0-CH6												S0-CH5(HI)							
S1-CH2 (LO)								S1-CH1												S1-CH0											
S1-CH5(LO)								S1-CH4								S1-CH3												S1-CH2(HI)			
S1-CH7												S1-CH6												S1-CH5(HI)							
….																															
S(N-1)-CH7												S(N-1)-CH6												S(N-1)-CH5(HI)							
S2-TR00 (LO)								S1-TR00												S0-TR00											
S5-TR00(LO)								S4-TR00								S3-TR00												S2-TR00(HI)			
S7-TR00												S6-TR00												S5-TR00(HI)							
….																															
S(N-1)- TR00												S(N-2)- TR00												S(N-3)- TR00(HI)							
31	30	TRIGGER TIME TAG																													

Fig. 3.13: Group Data Format

In the Group Event Description Word (yellow in the figure above) the following fields are shown:

- Bit [29:20] Start Index Cell of DRS4 related to this event
- Bit [17:16] (sampling frequency):
  - 00 = 5GS/s
  - 01 = 2.5GS/s
  - 10 = 1GS/s
  - 11 = not used
- Bit [12] (tr):
  - 0 = TRn signal not present in readout
  - 1 = TRn signal present in readout
- Bit [11:0] Size related to channel 0-7 (number of 32 bit words): when each channel has 1024 samples, “Size Ch 0-7” is 0xC00.

If readout of TRn is disabled, data related to such channel (light blue in figure above) are not present in the event; if readout of TRn is enabled, data size related to such channel is Size (TRn) = (Size Ch 0-7)/8.
Trigger Time Tag records the Trigger arrival time; each bin has a 8.5ns width.

3.6.1. Memory FULL management

Bit5 of Acquisition Control register (see § 4.23), allows to select Memory FULL management mode:

In Normal Mode the board becomes full, whenever all buffers are full; otherwise ("Always one buffer free" mode) it is possible to always keep one buffer free: board becomes full, whenever N-1buffers are full; with N = nr. of blocks.
In Normal Mode, the board waits until one buffer is filled since FULL status is exited (whether the trigger is overlapped or not). The board exits FULL status at the moment which the last datum from the last channel participating to the event is read.
In "Always one buffer free" mode, one buffer cannot be used (therefore it is NOT POSSIBLE, with this mode, to set Buffer Code to 0000; see § 4.19), but this allows to eliminate dead time when FULL status is exited.

3.7. Trigger management

Signal digitization can be triggered basically in two ways:

- **Common trigger**: a trigger produced via software (via VME or Optical Link) or sent via front panel TRG_IN signal (NIM/TTL signal on LEMO connector, 50 Ohm impedance.). In this case, all the channels in a board share the same trigger.
- **Low latency trigger**: a logic level fed directly into the DRS4 via the front panel TRn signals. In this case, one TRn signal triggers two groups (TR0 for Groups 0 and 1; TR1 for Groups 2 and 3)

As a trigger signal arrives, the ADC analog buffers related to that trigger, are frozen and then digitized with a 12bit resolution into the digital memory buffer.

During analog to digital conversion process, the V1742 cannot handles other triggers; this "Dead Time" is larger if also TR0 and/or TR1 input channels are sampled together with the analog inputs (see §3.3).

The TR0 and TR1 are actually analog inputs, but they are also TTL/NIM compatible; in order to use them as low latency external trigger signals, it is necessary to set properly the Configuration Register "Local TRn Trigger Enable" bit (see §3.3).

Once the acquisition is triggered in one of the ways described above, digitization takes place as described in § 3.2.

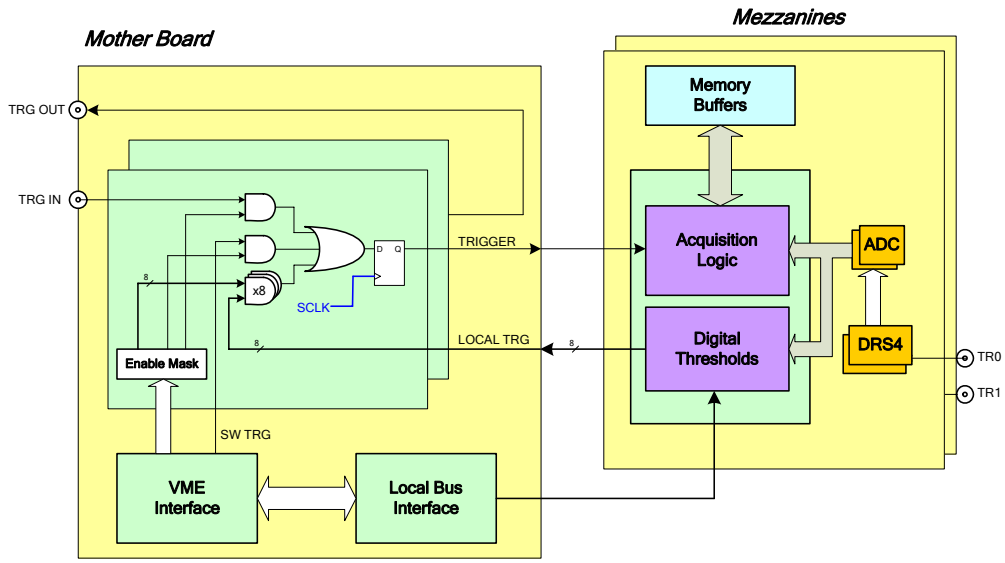

Fig. 3.14: Block diagram of Trigger management

3.7.1. Trigger distribution

The OR of all the enabled trigger sources, after being synchronized with the internal clock, becomes the global trigger of the board and is fed in parallel to all the channels, which store an event.
A Trigger Out is also generated on the relevant front panel TRG_OUT connector (NIM or TTL), and allows to extend the trigger signal to other boards.
For example, in order to start the acquisition on all the channels in the crate, as one of the channels ramps over threshold, the Local Trigger must be enabled as Trigger Out, the Trigger Out must then be fed to a Fan Out unit; the obtained signal has to be fed to the External Trigger Input of all the boards in the crate (including the board which generated the Trigger Out signal).

3.8. Front Panel I/Os

The V1742 is provided with 16 programmable general purpose LVDS I/O signals. Signals can be programmed via VME (see § 4.29 and § 4.30).
Default configuration is:

Table 3.1 : Front Panel I/Os default setting

Nr.	Direction	Description
0	out	Group 0 Trigger Request
1	out	Group 1 Trigger Request
2	out	Group 2 Trigger Request
3	out	Group 3 Trigger Request
4	-	-
5	-	-
6	-	-
7	-	-
8	out	Memory Full
9	out	Event Data Ready
10	out	Channels Trigger
11	out	RUN Status
12	in	Trigger Time Tag Reset (active low)
13	in	Memory Clear (active low)
14	-	RESERVED
15	-	RESERVED

3.9. Test pattern generator

The FPGA can emulate the ADC and write into memory a sawtooth signal for test purposes. It can be enabled via Group Configuration register, see § 4.16.
The following figure shows the test waveforms for even and odd groups respectively.

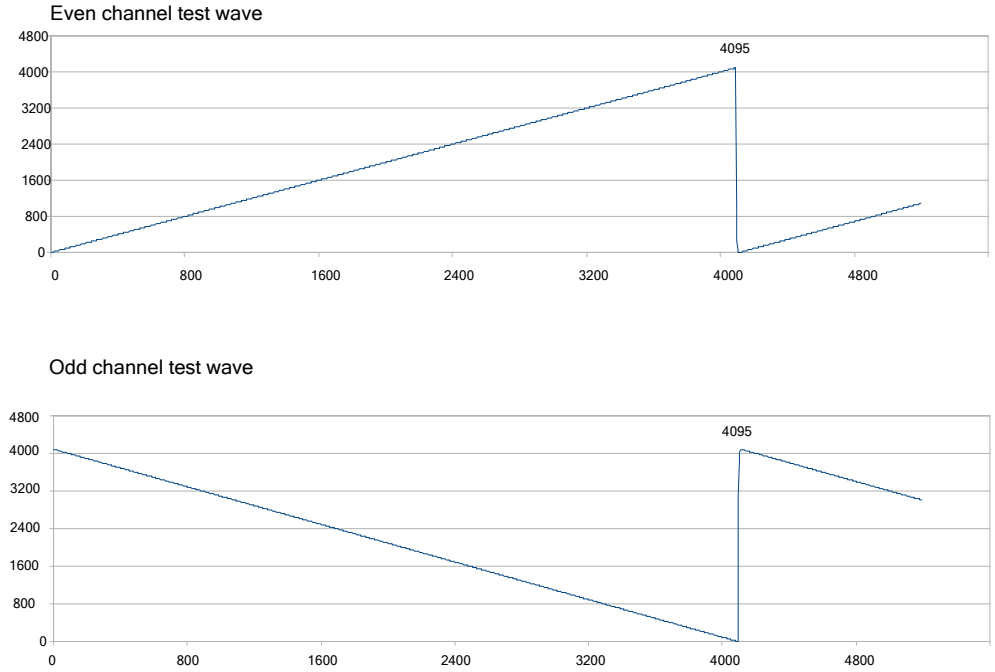

Fig. 3.15: FPGA test waveform

Since an event is made up of up to 1024 samples, the test event samples only a "portion" of the sawtooth; the start point of the sampling can be programmed via Initial Test Wave Value register (see § 4.21); for example if this register is set to 0x0FF then the channels in the even groups sample the ramp between 255 and 1278; the channels in the odd groups instead sample the complementary value, therefore between 3840 and 2817.

3.10. Reset, Clear and Default Configuration

3.10.1. Global Reset

Global Reset is performed at Power ON of the module or via a VME RESET (SYS_RES), see § 4.47. It allows to clear the data off the Output Buffer, the event counter and performs a FPGAs global reset, which restores the FPGAs to the default configuration. It initializes all counters to their initial state and clears all detected error conditions.

3.10.2. Memory Reset

The Memory Reset clears the data off the Output Buffer.
The Memory Reset can be forwarded via either a write access to Software Clear Register (see § 4.48) or with a pulse sent to the front panel Memory Clear input (see § 3.8).

3.10.3. Timer Reset

The Timer Reset allows to initialize the timer which allows to tag an event. The Timer Reset can be forwarded with a pulse sent to Trigger Time Tag Reset input (see § 3.8).

3.11. VMEBus interface

The module is provided with a fully compliant VME64/VME64X interface (see § 1.1), whose main features are:

- EUROCARD 9U Format
- J1/P1 and J2/P2 with either 160 pins (5 rows) or 96 (3 rows) connectors
- A24, A32 and CR-CSR address modes
- D32, BLT/MBLT, 2eVME, 2eSST data modes
- MCST write capability
- CBLT data transfers
- RORA interrupter
- Configuration ROM

3.11.1. Addressing capabilities

3.11.1.1. Base address

The module works in A24/A32 mode. The Base Address of the module can be fixed through four rotary switches (see § 2.6) and is written into a word of 24 or 32 bit.
The Base Address can be selected in the range:

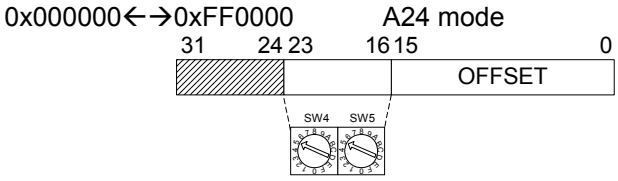

Fig. 3.16: A24 addressing

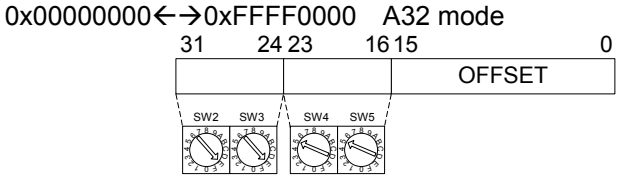

Fig. 3.17: A32 addressing

The Base Address of the module is selected through four rotary switches (see § 2.6), then it is validated only with either a Power ON cycle or a System Reset (see § 0).

3.11.1.2. CR/CSR address

GEO address is picked up from relevant backplane lines and written onto bit 23..19 of CR/CSR space, indicating the slot number in the crate; the recognized Address Modifier for this cycle is 2F. *This feature is implemented only on versions with 160pin connectors*.

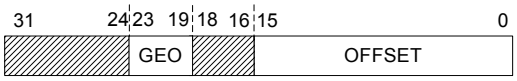

Fig. 3.18: CR/CSR addressing

3.11.1.3. Address relocation

Relocation Address register (see § 4.42) allows to set via software the board Base Address (valid values ≠ 0). Such register allows to overwrite the rotary switches settings; its setting is enabled via VME Control Register (see § 4.34). The used addresses are:

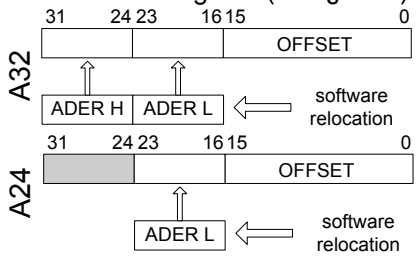

Fig. 3.19: Software relocation of base address

3.12. Data transfer capabilities

The board supports D32 single data readout, Block Transfer BLT32 and MBLT64, 2eVME and 2eSST cycles. Sustained readout rate is up to 60 MB/s with MBLT64, up to 100 MB/s with 2eVME and up to 160 MB/s with 2eSST.

3.13. Events readout

3.13.1. Sequential readout

The events, once written in the SRAMs (Memory Event Buffers), become available for readout via VME. During the memory readout, the board can continue to store more events (independently from the readout) on the free buffers. The acquisition process is therefore "deadtimeless", until the memory becomes full.
Although the memories are SRAMs, VMEBus does not handle directly the addresses, but takes them from a FIFO. Therefore, data are read from the memories sequentially, according to the selected Readout Logic, from a memory space mapped on 4Kbytes (0x0000÷0x0FFC).
The events are readout sequentially and completely, starting from the Header of the first available event, followed by the Trigger Time Tag, the Event Counter and all the samples of the channels (from 0 to 7). Once an event is completed, the relevant memory buffer becomes free and ready to be written again (old data are lost). After the last word in an event, the first word (Header) of the subsequent event is readout. It is not possible to readout an event partially.

3.13.1.1. SINGLE D32

This mode allows to readout a word per time, from the header (actually 4 words) of the first available event, followed by all the words until the end of the event, then the second event is transferred. The exact sequence of the transferred words is shown in § 3.5.
We suggest, after the 1st word is transferred, to check the Event Size information and then do as many D32 cycles as necessary (actually Event Size -1) in order to read completely the event.

3.13.1.2. BLOCK TRANSFER D32/D64, 2eVME

BLT32 allows, via a single channel access, to read N events in sequence, N is set via the BLT Event Number register (see § 4.45).

```
[Event Size] = [4*(Group Size)] + [16 bytes]
```

Group Size depends on Custom Size setting (see § 4.20) and whether TRn signals are stored in the event or not.
Then it is necessary to perform as many cycles as required in order to readout the programmed number of events.
We suggest to enable BERR signal during BLT32 cycles, in order to end the cycle avoiding filler readout. The last BLT32 cycle will not be completed, it will be ended by BERR after the #N event in memory is transferred (see example in the figure below).

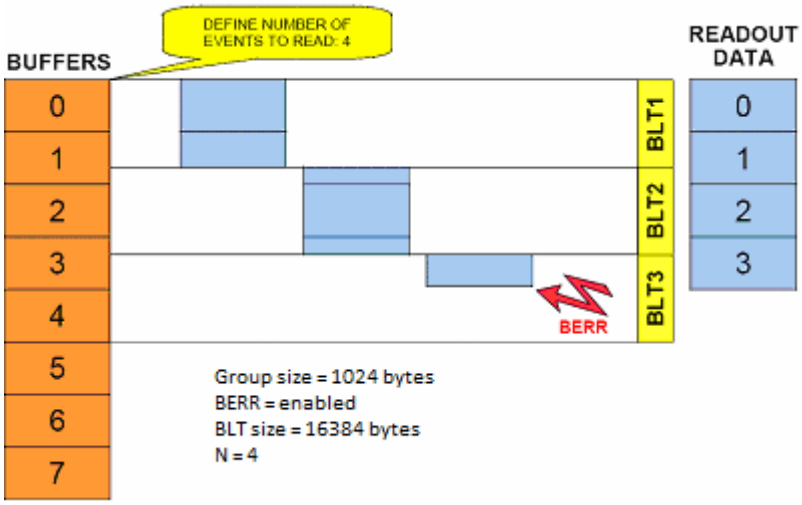

Fig. 3.20: Example of BLT readout

Since some 64 bit CPU's cut off the last 32 bit word of a transferred block, if the number of words composing such block is odd, it is necessary to add a dummy word (which has then to be removed via software) in order to avoid data loss. This can be achieved by setting the ALIGN64 bit in the VME Control register (see § 4.34).

MBLT64 cycle is similar to the BLT32 cycle, except that the address and data lines are multiplexed to form 64 bit address and data buses.

The 2eVME allows to achieve higher transfer rates thanks to the requirement of only two edges of the two control signals (DS and DTACK) to complete a data cycle.

3.13.1.3. CHAINED BLOCK TRANSFER D32/D64

The V1742 allows to readout events from more daisy chained boards (Chained Block Transfer mode). The technique which handles the CBLT is based on the passing of a token between the boards; it is necessary to verify that the used VME crate supports such cycles. Several contiguous boards, in order to be daisy chained, must be configured as “first”, “intermediate” or “last” via MCST Base Address and Control Register (see § 4.41). A common Base Address is then defined via the same register; when a BLT cycle is executed at the address CBLT_Base + 0x0000 ÷ 0x0FFC, the “first” board starts to transfer its data, driving DTACK properly; once the transfer is completed, the token is passed to the second board via the IACKIN-IACKOUT lines of the crate, and so on until the “last” board, which completes the data transfer and asserts BERR (which has to be enabled): the Master then ends the cycle and the slave boards are rearmed for a new acquisition.
If the size of the BLT cycle is smaller than the events size, the board which has the token waits for another BLT cycle to begin (from the point where the previous cycle has ended).

3.13.2. Event Polling

A read access to Event Size register (see § 4.36) allows “polling” the number of 32 bit words composing the next event to be read: this permits to perform a properly sized (according to the Event Size information) BLT readout from the Memory Event Buffer.

3.14. Optical Link

The board houses a daisy chainable Optical Link (communication path which uses optical fiber cables as physical transmission line) able to transfer data at 80 MB/s, therefore it is possible to connect up to eight V1742 to a single Optical Link Controller: for more information, see www.caen.it (path: Products / Front End / PCI/PCIe / Optical Controller)
The parameters for read/write accesses via optical link are the same used by VME cycles (Address Modifier, Base Address, data Width, etc); wrong parameter settings cause Bus Error.
VME Control Register bit 3 (see § 0) allows to enable the module to broadcast an interrupt request on the Optical Link; the enabled Optical Link Controllers propagate the interrupt on the PCI bus as a request from the Optical Link is sensed.
VME and Optical Link accesses take place on independent paths and are handled by board internal controller, with VME having higher priority; anyway it is better to avoid accessing the board via VME and Optical Link simultaneously.

3.15. Software tools

CAEN provides a library designed to control all kind of digitizer models: the CAENDigitizer, available for both Linux and Windows platform (32 and 64Bits).
The library is oriented to C/C++ programmers and for Labview developers.
The CAENDigitizer is in its turn implemented on a lower-level library, the CAENComm as described in the picture below:

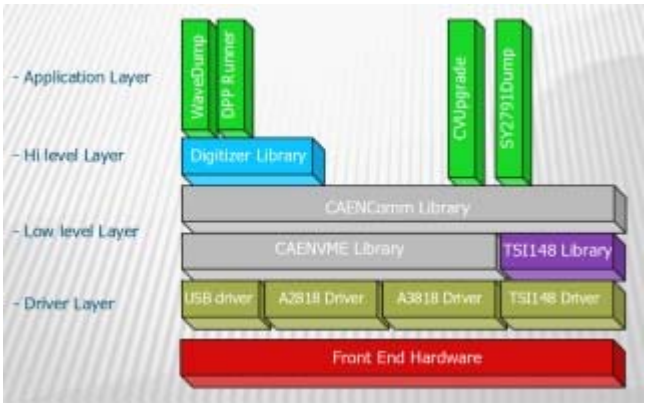

Fig. 3.21: Block diagram of the software tools

Demo software applications that use CAENDigitizer library and tools to upgrade the digitizers firmware (based on the CAENComm library) are also available; all demos and high-level programs are provided with their source code and can be used as a starting point for the development of User-specific applications.
For more information about the CAENDigitizer, the CAENComm and all the high-level software for this digitizer, please see www.caen.it website (Software download section).

4. VME Interface

The following sections will describe in detail the board's VME-accessible registers content.
Registers whose name begins with "Group n", are referred to channel groups, with index "n" in the address going from 0 to 3; each group is composed by eight subsequent channels.

⚠ N.B.: bit fields that are not described in the register bit map are reserved and must not be over written by the User.

4.1. Registers address map

Table 4.1: Address Map for the Model V1742

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT READOUT BUFFER	0x0000-0x0FFC	A24/A32/A64	D32	R	X	X	X
Group n Channel THRESHOLD	0x1n80	A24/A32	D32	R/W	X	X	
Group n STATUS	0x1n88	A24/A32	D32	R	X	X	
Daughter board FW revision	0x1n8C	A24/A32	D32	R			
Group n BUFFER OCCUPANCY	0x1n94	A24/A32	D32	R	X	X	X
Group n Channel DC offset	0x1n98	A24/A32	D32	R/W	X	X	
Group n DAC SEL	0x1nA4	A24/A32	D32	R / W	X	X	
DRS4 n Temperature	0x1nA0	A24/A32	D32	R	X	X	
Group n CHANNEL TRIGGER ENABLE MASK	0x1nA8	A24/A32	D32	R/W	X	X	
Memory Calibration Tables ENABLE	0x1nCC	A24/A32	D32	R/W	X	X	
Memory Calibration Tables DATA	0x1nD0	A24/A32	D32	R/W	X	X	
Group n TR THRESHOLD	0x1nD4	A24/A32	D32	R / W	X	X	
Group n TR DC offset	0x1nDC	A24/A32	D32	R / W	X	X	
Group CONFIGURATION	0x8000	A24/A32	D32	R/W	X	X	
Group CONFIGURATION BIT SET	0x8004	A24/A32	D32	W	X	X	
Group CONFIGURATION BIT CLEAR	0x8008	A24/A32	D32	W	X	X	
BUFFER ORGANIZATION	0x800C	A24/A32	D32	R/W	X	X	
CUSTOM SIZE	0x8020	A24/A32	D32	R/W	X	X	
INITIAL TEST WAVE	0x807C	A24/A32	D32	R/W	X	X	
SAMPLING FREQUENCY	0x80D8	A24/A32	D32	R/W	X	X	
ACQUISITION CONTROL	0x8100	A24/A32	D32	R/W	X	X	
ACQUISITION STATUS	0x8104	A24/A32	D32	R	X	X	
SW TRIGGER	0x8108	A24/A32	D32	W			
TRIGGER SOURCE ENABLE MASK	0x810C	A24/A32	D32	R/W	X	X	
FRONT PANEL TRIGGER OUT ENABLE MASK	0x8110	A24/A32	D32	R/W	X	X	
POST TRIGGER SETTING	0x8114	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O DATA	0x8118	A24/A32	D32	R/W	X	X	
FRONT PANEL I/O CONTROL	0x811C	A24/A32	D32	R/W	X	X	
Group ENABLE MASK	0x8120	A24/A32	D32	R/W	X	X	
ROC FPGA FIRMWARE REVISION	0x8124	A24/A32	D32	R			

REGISTER NAME	ADDRESS	ASIZE	DSIZE	MODE	H_RES	S_RES	CLR
EVENT STORED	0x812C	A24/A32	D32	R	X	X	X
SET MONITOR DAC	0x8138	A24/A32	D32	R/W	X	X	
BOARD INFO	0x8140	A24/A32	D32	R			
MONITOR MODE	0x8144	A24/A32	D32	R/W	X	X	
EVENT SIZE	0x814C	A24/A32	D32	R	X	X	X
VME CONTROL	0xEF00	A24/A32	D32	R/W	X		
VME STATUS	0xEF04	A24/A32	D32	R			
BOARD ID	0xEF08	A24/A32	D32	R/W	X	X	
MULTICAST BASE ADDRESS & CONTROL	0xEF0C	A24/A32	D32	R/W	X		
RELOCATION ADDRESS	0xEF10	A24/A32	D32	R/W	X		
INTERRUPT STATUS ID	0xEF14	A24/A32	D32	R/W	X		
INTERRUPT EVENT NUMBER	0xEF18	A24/A32	D32	R/W	X	X	
BLT EVENT NUMBER	0xEF1C	A24/A32	D32	R/W	X	X	
SCRATCH	0xEF20	A24/A32	D32	R/W	X	X	
SW RESET	0xEF24	A24/A32	D32	W			
SW CLEAR	0xEF28	A24/A32	D32	W			
FLASH ENABLE	0xEF2C	A24/A32	D32	R/W	X		
FLASH DATA	0xEF30	A24/A32	D32	R/W	X		
CONFIGURATION RELOAD	0xEF34	A24/A32	D32	W			
CONFIGURATION ROM	0xF000-0xF3FC	A24/A32	D32	R			

4.2. Configuration ROM (0xF000-0xF084; r)

The following registers contain some module's information, they are D32 accessible (read only):

- **OUI**: manufacturer identifier (IEEE OUI)
- **Version**: purchased version
- **Board ID**: Board identifier
- **Revision**: hardware revision identifier
- **Serial MSB**: serial number (MSB)
- **Serial LSB**: serial number (LSB)

Table 4.2: ROM Address Map for the Model V1742

Description	Address	Content
checksum	0xF000	*0xA4*
checksum_length2	0xF004	0x00
checksum_length1	0xF008	0x00
checksum_length0	0xF00C	0x20
constant2	0xF010	0x83
constant1	0xF014	0x84
constant0	0xF018	0x01
c_code	0xF01C	0x43
r_code	0xF020	0x52
oui2	0xF024	0x00
oui1	0xF028	0x40
oui0	0xF02C	0xE6
vers	0xF030	V1742, VX1742: 0x70
board2	0xF034	V1742: 0x00; VX1742: 0x01
board1	0xF038	0x06
board0	0xF03C	0xCE
revis3	0xF040	*0x00*
revis2	0xF044	*0x00*
revis1	0xF048	*0x00*
revis0	0xF04C	*0x01*
sernum1	0xF080	*0x00*
sernum0	0xF084	*0x16*

These data are written into one Flash page; at Power ON the Flash content is loaded into the Configuration RAM, where it is available for readout.

4.3. Group n Channel Threshold (0x1n80; r/w)

Bit	Function
[31:0]	*reserved*

4.4. Group n Status (0x1n88; r)

Bit	Function
[8]	DRS Chips Busy
[7]	Group Odd PLL Lock
[6]	Group Even PLL Lock
[5]	*reserved*
[4]	Group Odd Enable
[3]	Group Even Enable
[2]	SPI Bus Busy: 1 = Busy 0 = SPI ready
[1]	Memory empty
[0]	Memory full

4.5. Daughter board FW revision (0x1n8C; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).
Example: revision 1.3 of 12th June 2010 is: 0xA6120103

4.6. Group n Buffer Occupancy (0x1n94; r)

Bit	Function
[10:0]	Occupied buffers (0..1024)

4.7. Group n Channel DC offset (0x1n98; r/w)

Bit	Function
[19:16]	Channel index from 0x0 to 0x7 (only one DAC ch.) or 0xF (all DAC ch.)
[15:0]	DAC Data

The input DC offset can be adjusted group per group and channel per channel by means of a programmable 16bit DAC; there is a DAC serving each group (8 channels).
Default value 0x8F00 (about 0mV, for input bipolar signals.)
The channel index field (bits [19:16]) is used only in write access. In read access, channel index must be set on CH DAC SEL register (see Channel DAC Select register).
For example, in order to set the DAC Value 0x6C00 for channel 15 (channel 7 of group 1) a write access to address 0x1198 with value 0x76C00 must be performed.
In order to readout the channel 15 DAC Value, a write access to address 0x11A4 with value 0x7 must be performed, and then a read access to address 0x1198.

4.8. Group n ADC Configuration (0x1n9C; r/w)

Bit	Function
[31:0]	*reserved*

4.9. DRS4 temperature (0x1nA0; r)

Bit	Function
[7:0]	DRS4 temperature from 0°C to 127°C

4.10. Channel n DAC SEL (0x1nA4; r/w)

Bit	Function
[3:0]	DAC Channel index for readout, from 0x0 to 0x7.

For example, in order to read the channel 15 DAC Value, a write access to address 0x11A4 with value 0x7 (channel 15 is channel 7 of group 1) must be performed, and then a read access to address 0x1198.

4.11. Group n Channel Trigger Mask (0x1nA8; r/w)

Bit	Function
[31:0]	*reserved*

4.12. Memory Calibration Tables Enable (0x1nCC; r/w)

Bit	Function
0	0 = Memory Calibration Tables ENABLED 1 = Memory Calibration Tables DISABLED

This register allows to access the memory location where calibration data are stored (see § 3.5). CAUTION: before writing this register it is necessary to verify that SPI Bus Busy Flag in the Status register (§ 4.4) is 0 and, in any case, its use is reserved to experienced Users, since a wrong value written in the Memory Calibration Data will erase the module's calibration pattern.

4.13. Memory Calibration Tables Data (0x1nD0; r/w)

Bit	Function
[7:0]	Data to be serialized or read from Memory Tables calibration

This register allows to access the memory location where calibration data are stored (see § 3.5). CAUTION: before writing this register it is necessary to verify that SPI Bus Busy Flag in the Status register (§ 4.4) is 0 and, in any case, its use is reserved to experienced Users, since a wrong value written in the Memory Calibration Data will erase the module's calibration pattern.

4.14. Group n TR Threshold (0x1nD4; r/w)

Bit	Function
[15:0]	Threshold

The threshold on TRn for local trigger generation can be set by a programmable 16bit DAC. One TRn signal is common to two groups, therefore, for example write access to either 0x10D4 or 0x11D4 leads to the same setting for TR0 input.
For TRn Threshold setting example, see the paragraph below.

4.15. Group n TR DC offset (0x1nDC; r/w)

Bit	Function
[15:0]	DC Offset

The TRn signal offset can be set by means of a programmable 16bit DAC.
For example, in order to set the TR0 (signal common to groups 0 and 1) DC offset value to 0x6C00 a write access to address 0x10DC with value 0x56C00 must be performed. One TR signal is common to two groups, therefore, for example write access to either 0x10DC or 0x11DC leads to the same setting.

Level setting example:
If you are working with TRn NIM signal:

TR0 DC Offset = 0x1000 (write 0x1000 at address 0x10DC or 0x11DC)
TR0 Threshold = 0x7300 (write 0x7300 at address 0x10D4 or 0x11D4)
TR1 DC Offset = 0x1000 (write 0x1000 at address 0x12DC or 0x13DC)
TR1 Threshold = 0x7300 (write 0x7300 at address 0x12D4 or 0x13D4)

If you are working with TRn TTL signal:
TR0 DC Offset = 0x4000 (write 0x4000 at address 0x10DC or 0x11DC)
TR0 Threshold = 0x7300 (write 0x7300 at address 0x10D4 or 0x11D4)
TR1 DC Offset = 0x4000 (write 0x4000 at address 0x12DC or 0x13DC)
TR1 Threshold = 0x7300 (write 0x7300 at address 0x12D4 or 0x13D4)

4.16. Group Configuration Register (0x8000; r/w)

Bit	Function
[31:28]	Select monitor signal from daughter board 0000= no signal 0001= all fast trigger 0010= accepted fast trigger 0011= busy
[27:13]	*reserved* (MUST ALWAYS BE SET TO 0)
[12]	TRn Trigger Enable: when this bit is 1, TRn signal is used as local trigger: 0= TRn Local Trigger disabled (Default) 1= TRn Local Trigger enabled
[11]	Signal TRn Readout Enable: when this bit is 1, signal TRn is present in data readout: 0= Signal TRn Readout disabled (Default) 1= Signal TRn Readout enabled
[10:9]	*reserved* (MUST ALWAYS BE SET TO 0)
[8]	Individual Trigger: must be 1
[7]	*reserved* (MUST ALWAYS BE SET TO 0)
[6]	TR Trigger polarity: 0= Rising Edge (Default) 1= Falling Edge.
[5]	*reserved* (MUST ALWAYS BE SET TO 0)
[4]	*reserved* (MUST ALWAYS BE SET TO 1)
[3]	Test Mode: when this bit is 1, the ADC samples are replaced by a sawtooth generated by the FPGA 0= Normal mode (data from the DRS4 and ADC, Default) 1= Test Mode (emulated data: from the sawtooth generator)
[2:0]	*reserved* (MUST ALWAYS BE SET TO 0)

There are three ways to write the content of the Configuration Register:

- Normal Write (at address 0x8000): the content of the register is fully overwritten by the new data.
- Bit Set Mode (at address 0x8004): writing '1' in one bit, will set that bit; writing '0' leaves the bit unchanged.
- Bit Clear Mode (at address 0x8008): writing '1' in one bit, will clear that bit; writing '0' leaves the bit unchanged.

The use of the Bit Set/Clear modes are recommended when concurrent processes can access the register; this prevents a process to operate on the content of the register while another process has already changed it. The read access to the Control Register can be done at 0x8000 address.

4.17. Group Configuration Bit Set (0x8004; w)

Bit	Function
[31:0]	Bits set to 1 means that the corresponding bits in the Group Configuration register are set to 1.

4.18. Group Configuration Bit Clear (0x8008; w)

Bit	Function
[31:0]	Bits set to 1 means that the corresponding bits in the Group Configuration register are set to 0.

4.19. Buffer Organization (0x800C; r/w)

Bit	Function
[31:0]	*reserved* (always set to 0)

4.20. Custom Size (0x8020; r/w)

Bit	Function
[1:0]	00= 1024 sample/ch 01= 520 sample/ch 10= 256 sample/ch 11= 136 sample/ch

This register must not be written while acquisition is running.

4.21. Initial test wave value (0x807C)

Bit	Function
[11:0]	Test wave start value

4.22. Sampling Frequency (0x80D8)

Bit	Function
[1:0]	00 = 5 GS/s 01 = 2.5 GS/s 10 = 1 GS/s 11 = *reserved* (do not use)

This register must not be written while acquisition is running.

4.23. Acquisition Control (0x8100; r/w)

Bit	Function
[5]	0 = Normal Mode (default): board becomes full, whenever all buffers are full (see § 4.19) 1 = Always keep one buffer free: board becomes full, whenever N-1 buffers are full; N = nr. of blocks (see § 4.19)
[4]	*reserved*
[3]	0 = COUNT ACCEPTED TRIGGERS 1 = COUNT ALL TRIGGERS allows to reject overlapping triggers (see § 3.5)
[2]	0 = Acquisition STOP 1 = Acquisition RUN allows to RUN/STOP Acquisition
[1:0]	*reserved*

Bit [2] allows to Run and Stop data acquisition; when such bit is set to 1 the board enters Run mode and a Memory Reset (see § 3.10.2) is automatically performed. When bit [2] is reset to 0 the stored data are kept available for readout. In Stop Mode all triggers are neglected.

4.24. Acquisition Status (0x8104; r)

Bit	Function
[8]	Board ready for acquisition (PLL and ADCs are synchronized correctly) 0 = not ready 1 = ready This bit should be checked after software reset to ensure that the board will enter immediately run mode after RUN mode setting; otherwise a latency between RUN mode setting and Acquisition start might occur.
[7]	PLL Status Flag (see § 2.5.1): 0 = PLL loss of lock 1 = no PLL loss of lock NOTE: flag can be restored to 1 via read access to Status Register (see § 4.39)
[6]	PLL Bypass mode (see § 2.5.1): 0 = No bypass mode 1 = Bypass mode
[5]	Clock source (see § 2.6): 0 = Internal 1 = External
[4]	EVENT FULL: it is set to 1 as the maximum nr. of events to be read is reached
[3]	EVENT READY: it is set to 1 as at least one event is available to readout
[2]	0 = RUN off 1 = RUN on
[1:0]	*reserved*

4.25. Software Trigger (0x8108; w)

Bit	Function
[31:0]	A write access to this location generates a trigger via software

4.26. Trigger Source Enable Mask (0x810C; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:0]	*reserved*

EXTERNAL TRIGGER ENABLE (bit30) enables the board to accept the TRG_IN
SW TRIGGER ENABLE (bit 31) enables the board to accept the software trigger (see § 4.25).

4.27. Front Panel Trigger Out Enable Mask (0x8110; r/w)

Bit	Function
[31]	0 = Software Trigger Disabled 1 = Software Trigger Enabled
[30]	0 = External Trigger Disabled 1 = External Trigger Enabled
[29:4]	*reserved*
[3]	0 = Group 3 trigger disabled 1 = Group 3 trigger enabled
[2]	0 = Group 2 trigger disabled 1 = Group 2 trigger enabled
[1]	0 = Group 1 trigger disabled 1 = Group 1 trigger enabled
[0]	0 = Group 0 trigger disabled 1 = Group 0 trigger enabled

This register bits[3:0] enable the groups to generate a trigger as the relevant TRn signal signal (TR0 for group 0, 1 and TR1 for group 2, 3) exceeds the set threshold (see § 4.12).
EXTERNAL TRIGGER ENABLE (bit30) enables the board to generate the TRG_OUT.
SW TRIGGER ENABLE (bit 31) enables the board to broadcast a software trigger (see § 4.25).

4.28. Post Trigger Setting (0x8114; r/w)

Bit	Function
[31:0]	Size of the post trigger window

The register value sets the size of the post trigger window (expressed in step of about 8.5ns); the maximum value for the post trigger is 0x7F.

4.29. Front Panel I/O Data (0x8118; r/w)

Bit	Function
[15:0]	Front Panel I/O Data

Allows to Readout the logic level of LVDS I/Os and set the logic level of LVDS Outputs.

4.30. Front Panel I/O Control (0x811C; r/w)

Bit	Function
[15]	0 = I/O Normal operations: TRG-OUT signals outside trigger presence (trigger are generated according to Front Panel Trigger Out Enable Mask setting, see § 4.26) 1= I/O Test Mode: TRG-OUT is a logic level set via bit 14
[14]	1= TRG-OUT Test Mode set to 1 0 = TRG-OUT Test Mode set to 0
[13:8]	*reserved*
[7:6]	00 = General Purpose I/O 01 = Programmed I/O 10 = Pattern mode: LVDS signals are input and their value is written into header PATTERN field
[5]	0 = LVDS I/O 15..12 are inputs 1 = LVDS I/O 15..12 are outputs
[4]	0 = LVDS I/O 11..8 are inputs 1 = LVDS I/O 11..8 are outputs
[3]	0 = LVDS I/O 7..4 are inputs 1 = LVDS I/O 7..4 are outputs
[2]	0 = LVDS I/O 3..0 are inputs 1 = LVDS I/O 3..0 are outputs
[1]	0= panel output signals (TRG-OUT/CLKOUT) enabled 1= panel output signals (TRG-OUT/CLKOUT) enabled in high impedance
[0]	0 = TRG/CLK are NIM I/O Levels 1 = TRG/CLK are TTL I/O Levels

Bits [5:2] are meaningful for General Purpose I/O use only

4.31. Group Enable Mask (0x8120; r/w)

Bit	Function
[3]	0 = Group 3 disabled 1 = Group 3 enabled
[2]	0 = Group 2 disabled 1 = Group 2 enabled
[1]	0 = Group 1 disabled 1 = Group 1 enabled
[0]	0 = Group 0 disabled 1 = Group 0 enabled

Enabled groups provide the samples which are stored into the events (and not erased). The mask cannot be changed while acquisition is running.

4.32. ROC FPGA Firmware Revision (0x8124; r)

Bit	Function
[31:16]	Revision date in Y/M/DD format
[15:8]	Firmware Revision (X)
[7:0]	Firmware Revision (Y)

Bits [31:16] contain the Revision date in Y/M/DD format.
Bits [15:0] contain the firmware revision number coded on 16 bit (X.Y format).

4.33. Event Stored (0x812C; r)

Bit	Function
[31:0]	This register contains the number of events currently stored in the Output Buffer

This register value cannot exceed the maximum number of available buffers according to setting of buffer size register.

4.34. Set Monitor DAC (0x8138; r/w)

Bit	Function
[31:0]	*reserved*

4.35. Board Info (0x8140; r)

Bit	Function
[15:8]	Memory size (Mbyte/Group)
[7:0]	Board Type: 0x06

4.36. Monitor Mode (0x8144; r/w)

Bit	Function
[31:0]	*reserved*

4.37. Event Size (0x814C; r)

Bit	Function
[31:0]	Nr. of 32 bit words in the next event

4.38. VME Control (0xEF00; r/w)

Bit	Function
[7]	0 = Release On Register Access (RORA) Interrupt mode (default) 1 = Release On AcKnowledge (ROAK) Interrupt mode
[6]	0 = RELOC Disabled (BA is selected via Rotary Switch; see § 2.6) 1 = RELOC Enabled (BA is selected via RELOC register; see § 4.42)
[5]	0 = ALIGN64 Disabled 1 = ALIGN64 Enabled (see § 3.13.1.2)
[4]	0 = BERR Not Enabled; the module sends a DTACK signal until the CPU inquires the module 1 = BERR Enabled; the module is enabled either to generate a Bus error to finish a block transfer or during the empty buffer read out in D32
[3]	0 = Optical Link interrupt disabled 1 = Optical Link interrupt enabled
[2 :0]	Interrupt level (0= interrupt disabled)

Bit [7]: this setting is valid only for interrupts broadcasted on VMEbus; interrupts broadcasted on optical link feature RORA mode only.

- In RORA mode, interrupt status can be removed by accessing VME Control register (see § 0) and disabling the active interrupt level.
- In ROAK mode, interrupt status is automatically removed via an interrupt acknowledge cycle.

Interrupt generation is restored by setting an Interrupt level > 0 via VME Control register.

4.39. VME Status (0xEF04; r)

Bit	Function
[3]	0 = VME FIFO not empty; 1 = VME FIFO empty
[2]	0 = BERR FLAG: no Bus Error has occurred 1 = BERR FLAG: a Bus Error has occurred (this bit is re-set after a status register read out)
[1]	*reserved*
[0]	0 = No Data Ready; 1 = Event Ready

4.40. Board ID (0xEF08; r/w)

Bit	Function
[4:0]	GEO

- VME64X versions: this register can be accessed in read mode only and contains the GEO address of the module picked from the backplane connectors; when CBLT is performed, the GEO address will be contained in the EVENT HEADER Board ID field.
- Other versions: this register can be accessed both in read and write mode; it allows to write the correct GEO address (default setting = 0) of the module before CBLT operation. GEO address will be contained in the EVENT HEADER Board ID field.

4.41. MCST Base Address and Control (0xEF0C; r/w)

Bit	Function
[9:8]	Allows to set up the board for daisy chaining: 00 = disabled board 01 = last board 10 = first board 11 = intermediate
[7:0]	These bits contain the most significant bits of the MCST/CBLT address of the module set via VME, i.e. the address used in MCST/CBLT operations.

4.42. Relocation Address (0xEF10; r/w)

Bit	Function
[15:0]	These bits contains the A31...A16 bits of the address of the module: it can be set via VME for a relocation of the Base Address of the module.

4.43. Interrupt Status ID (0xEF14; r/w)

Bit	Function
[31:0]	This register contains the STATUS/ID that the module places on the VME data bus during the Interrupt Acknowledge cycle

4.44. Interrupt Event Number (0xEF18; r/w)

Bit	Function
[9:0]	INTERRUPT EVENT NUMBER

If interrupts are enabled, the module generates a request whenever it has stored in memory a Number of events > INTERRUPT EVENT NUMBER

4.45. BLT Event Number (0xEF1C; r/w)

Bit	Function
[7:0]	This register defines the maximum number of events that can be transferred in a Block Transfer Cycle, after which the board asserts the Bus Error to stop the transfer. Allowed setting is between 0 (meaning no limit) and 255.

4.46. Scratch (0xEF20; r/w)

Bit	Function
[31:0]	Scratch (*to be used to write/read words for VME test purposes*)

4.47. Software Reset (0xEF24; w)

Bit	Function
[31:0]	A write access to this register causes a board reset (the acquisition is stopped, all the registers are set to the default settings and all data are cleared).

4.48. Software Clear (0xEF28; w)

Bit	Function
[31:0]	A write access to this register causes a data clear (the registers setting is not modified).

4.49. Flash Enable (0xEF2C; r/w)

Bit	Function
0	0 = Flash write ENABLED 1 = Flash write DISABLED

This register is handled by the Firmware upgrade tool.

4.50. Flash Data (0xEF30; r/w)

Bit	Function
[7:0]	Data to be serialized towards the SPI On board Flash

This register is handled by the Firmware upgrade tool.

4.51. Configuration Reload (0xEF34; w)

Bit	Function
[31:0]	A write access to this register causes a software reset (see § 0), a reload of Configuration ROM parameters and a PLL reconfiguration.

5. Installation

- The Mod. V1742 fits into all 6U VME crates.
- VX1742 versions require VME64X compliant crates
- Use only crates with forced cooling air flow
- Turn the crate OFF before board insertion/removal
- Remove all cables connected to the front panel before board insertion/removal

CAUTION

USE ONLY CRATES WITH FORCED COOLING AIR FLOW SINCE OVERHEAT MAY DAMAGE THE MODULE!

CAUTION

ALL CABLES MUST BE REMOVED FROM THE FRONT PANEL BEFORE EXTRACTING THE BOARD FROM THE CRATE!

5.1. Power ON sequence

To power ON the board follow this procedure:

1. insert the V1742 board into the crate
2. power up the crate

5.2. Power ON status

At power ON the module is in the following status:

- the Output Buffer is cleared;
- registers are set to their default configuration (see § 0)

5.3. Firmware upgrade

CAEN provides a firmware upgrade tool that can be used with either VME or optical link paths. Download the software package, application notes and user manual available at www.caen.it website (path: Products/FrontEnd/VME/Digitizer/ V1742)
then follow the instructions for installation and usage.

WARNING: in case of programming failures, the board can store two firmware versions, called STD and BKP respectively; at Power On, a microcontroller reads the Flash Memory and programs the module with the firmware version selected via the JP2 jumper (see § 2.6), which can be placed either on the STD position (left), or in the BKP position (right).
Please contact CAEN at support.frontend@caen.it for instructions in order to restore the backup image.
Once the board is successfully powered with backup firmware, the standard firmware image can be reprogrammed.